REMARKS

This paper is responsive to a final Office action dated December 16, 2003. The Office examined claims 1-33, and rejected all examined claims. Additionally, the Office objected to informalities in claims 13 and 14.

Claim Objections

Claims 13 and 14 have been amended to correct the informalities noted by the Examiner in the official action. No new matter was added by these amendments.

Claim Rejections under 35 USC Section 102

Claims 1-13 and 26-30

Claims 1-13 and 26-30 were rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent No. 6,212,599, issued to Baweja et al., hereinafter "Baweja".

Claim 1

In response to the applicant's previous remarks regarding the contents of Baweja, the Office indicated that the clock enable signal provided by first memory controller 210 (SDKE 240) during normal operation and the clock enable signal provided by suspend memory controller 220 (SCKE) satisfy the elements recited in claim 1 requiring a memory control signal to be supplied from one circuit according to an operational state, and supplied from another circuit during a power savings state. In support of these remarks, the Office points to Fig. 3 of Baweja and to the accompanying description of Fig. 3 in column 5 lines 1 through 22.

The relied upon portions of Baweja describe AND gate 320 having two inputs, SDCKE 240 and SCKE, which produces a clock enable signal CKE 330 when both inputs are high. Thus, rather than being supplied from a first location during an operational state and from another location during a power savings state, Baweja discloses that the clock enable signal CKE 330 is always supplied from the same location by the same circuit. The applicant respectfully notes that although partial control of the clock enable signal CKE 330 is provided by first

memory controller 210 during an operational state, the clock enable signal itself is supplied from suspend memory controller 220 under both operating and power savings states.

Because Baweja does not teach or suggest supplying a memory control signal from a first integrated circuit according to an operational state and from another location in a self refresh state, the applicant submits that Baweja does not teach or suggest each and every element of independent claim 1. Consequently, Baweja cannot support a rejections under 35 USC 102(e). The applicant, therefore, respectfully requests the Office to withdraw its rejection of claim 1 as being anticipated by Baweja, and allow claim 1 to issue.

Claims 2-7

Claims 2-7 depend, either directly or indirectly, from independent claim 1. Inasmuch as independent claim 1 is allowable, claims 2-7 are themselves allowable for at least that reason. The applicant, therefore, respectfully requests the Office to withdraw its rejection of claims 2-7, and allow claims 2-7 to issue.

Claim 8

Claim 8 recites isolating a first integrated circuit from memory during a power savings state. The Office's apparent position is that using state machine 310 to maintain the output of AND gate 320 at a low-level during a power savings state discloses isolating a first integrated circuit from memory during a power savings state. (See p. 9, response to item 10. *i.* (b) of the most recent official action.)

The applicant respectfully submits that AND gate 320, illustrated in Fig. 3 of Baweja, does not isolate the integrated circuit (i.e. memory system controller 200 of FIG. 2) from memory during the power savings state. In fact, clock enable signal CKE 330 is provided by suspend memory controller 220, which is part of memory system controller 200, during both an operational state and a low power state. This necessarily implies that memory system controller 200 is not isolated from the memory.

Because Baweja does not teach or suggest isolating a first integrated circuit from a memory during a power savings state, the applicant submits that Baweja does not teach or

suggest each and every element of independent claim 8. Consequently, the applicant submits that Baweja cannot support a rejections under 35 USC 102(e). The applicant, therefore, respectfully requests the Office to withdraw its rejection of claim 8 as being anticipated by Baweja, and allow claim 8 to issue.

Claim 9

Claim 9 recites that isolating a first integrated circuit from memory during a power savings state includes disabling a switch coupling the memory control signal from the first integrated circuit to the memory. The switch is disabled by driving a switch enable signal to turn off the switch.

The Office points to Fig. 2 and column 5, lines 16-22 of Baweja as inherently disclosing the elements recited in original claim 9. The Manual of Patent Examining Procedure states, "to serve as an anticipation when the reference is silent about the asserted inherent element, such gap in the reference may be filled with recourse to extrinsic evidence. Such evidence must make clear that the missing descriptive matter is *necessarily present* in the thing described in the reference, and that it would be so recognized by persons of ordinary skill." MPEP section 2131.01, paragraph III, citing *Continental Can Co. USA v. Monsanto Co.*, 948 F.2d 1264, 1268, 20 USPQ2d 1746, 1749 (Fed. Cir. 1991).

The applicant respectfully submits that a switch coupling the memory control signal from the first integrated circuit to the memory is not disclosed in Baweja. Neither does the record include evidence to indicate that such a switch is necessarily present in Baweja. Since claim 9 recites a switch coupling the memory control signal from the first integrated circuit, the applicant respectfully requests the office to provide evidence showing that such a switch is necessarily present in Baweja, or to withdraw its rejection of claim 9 and to allow this claim to issue.

Claim 10

Claim 10 recites a method including driving a signal line coupled to the switch and to the memory control signal input at a high impedance during an operational state.

The Office takes the position that the signal line carrying memory control signal CKE 260 (Baweja, Fig. 2) corresponds to the claimed signal line. (*See* Official Action, p. 5.) Assuming for the moment that this interpretation is correct, the method of claim 10 would drive the signal line carrying memory control signal CKE 260 to a predetermined logical level during a power savings state, and at a high impedance during an operational state. This interpretation of Baweja would result in the signal line carrying CKE 260 being effectively disconnected (driven at a high impedance) at a time when the first memory controller 210 is supposed to be controlling the memory control signal CKE 260.

The applicant respectfully submits that the signal line carrying CKE 260 cannot be equated with the signal line recited in claim 10, because, to do so, would render Baweja inoperable. For at least this reason, the applicant respectfully requests the Office to withdraw its rejection of claim 10, and allow this claim to issue.

Claims 11-12

The applicant submits that claims 11 and 12 each depend, either directly or indirectly, from allowable independent claim 8, and that claims 11 and 12 are allowable for at least this reason. The applicant, therefore, respectfully requests the Office to withdraw its rejection of claims 11 and 12, and allow these claims to issue.

Claim 26

Claim 26 has been amended to include the limitations previously recited in claims 29 and 30. In particular, claim 26 recites a method wherein an asserted reset signal holds a memory control signal at a first value in the first integrated circuit during the power savings state.

The Office states on page 4 of the official action, in reference to claims 29 and 30, that Baweja discloses holding the memory control signal at a first value to keep the memory into a refresh state. The Office further states on p. 10 of the official action, in responding to item 10 *i.* (f), that the clock enable signal SCKE disclosed in Baweja is a reset signal. The applicant respectfully submits that Baweja discloses clock enable signal SCKE as being a clock enable signal, and not a reset signal.

Inasmuch as Baweja does not disclose a method wherein an asserted reset signal holds a memory control signal at a first value in the first integrated circuit during the power savings state, as recited in independent claim 26, Baweja does not teach or suggest each and every element of claim 26. The applicant, therefore, respectfully requests the Office to withdraw its rejection of claim 26, and allow this claim to issue.

Claims 27-30

Claim 27 depends from the allowable independent claim 26. For at least this reason, the applicant submits that claim 27 is itself allowable, and respectfully requests the Office to withdraw its rejection of claim 27, and allow claim 27 to issue. Claims 28-30 have been canceled, and the elements recited in claims 29 and 30 have been incorporated into independent claim 26.

Claims 14-25 and 31

Claims 14-25 and 31 have been rejected under 35 U.S.C. 102(e) as being anticipated Baweja. Specifically, the Office stated that these claims encompass the same scope of invention as that of claims 1-13, and rejected claims 14-25 and 31 for that reason.

Claim 14

Claim 14 recites, "a memory control circuit coupled to the system memory to provide a memory control signal during an operational state, and a second circuit, independent of the memory control circuit, coupled to cause the memory control signal to be at the first value during a power savings state."

In the applicant's response to the previous official action, the applicant asserted that Fig. 2 of Baweja disclosed a suspend memory controller 220 supplying clock enable signal CKE 260 during both an operational state and a power savings state, thereby failing to disclose a second, independent memory control circuit. On p. 9 of the official action, in responding to item 10 *i.* (c), the Office refers to Fig. 3, col. 5, lines 19-22, to rebut the applicant's assertion that Baweja does not disclose an independent memory control circuit coupled to cause the memory control signal to be at the first value during a power savings state.

The applicant refers the Office to Baweja, col. 4, lines 32-34, which states, "during normal operation, the suspend memory controller 220 acts as part of the memory system controller 200." The applicant submits, that memory system controller 200 supplies the clock enable signal using both first memory controller 210 and suspend memory controller 220 during an operational state, and that memory system controller 200 supplies the clock enable signal using suspend memory controller 220 during a low-power state. Thus, a single portion of the memory system controller 200, namely suspend memory controller 220, supplies the clock enable signal during both operational and low-power states. (See, Baweja, Figs. 2 and 3 and their accompanying descriptions.)

For at least this reason, the applicant submits that Baweja does not teach or suggest each and every element recited in claim 14, and respectfully requests the Office to withdraw its rejection of claim 14 and allow claim 14 to issue.

Claim 15

Claim 15 recites the computer system, as recited in claim 14, further comprising an isolation circuit coupled between the memory control circuit and the memory. The applicant respectfully submits that the Office has not shown any portion of Baweja that teaches or suggests an isolation circuit. Additionally, inasmuch as claim 15 depends from allowable independent claim 14, the applicant submits that claim 15 is itself allowable. For at least these reasons, the applicant respectfully requests the Office to withdraw its rejection of claim 15, and allow claim 15 to issue.

Claim 16

Claim 16 recites that the second circuit, independent of the memory control circuit, is coupled to provide a high impedance on an output terminal. Claim 16 further recites that during an operational state of the computer system the output terminal is coupled to the isolation circuit and the memory to provide a memory control signal, and that the second circuit is coupled to drive the output terminal and thereby the memory control signal to low voltage level during the power savings state.

The Office has pointed to nothing in Baweja that shows that a second circuit, independent of a memory control circuit, is coupled to provide a high impedance on an output terminal. Additionally, inasmuch as claim 16 depends, either directly or indirectly from an allowable independent claim 14, the applicant submits that claim 16 is itself allowable. For at least these reasons, the applicant respectfully requests the Office to withdraw its rejection of claim 16, and allow claim 16 to issue.

Claim 17

Claim 17 recites that the second circuit, independent of the memory control circuit, is coupled to provide an isolation control signal to the isolation circuit during a power savings state to isolate the memory control signal from the memory control circuit during a power savings state.

Notwithstanding the Office's position that isolating the memory control circuit from the memory during a low-power state is inherently disclosed in Baweja, the Office has pointed to nothing in Baweja that shows that a second circuit, independent of a memory control circuit, is coupled to provide an isolation control signal to an isolation circuit. Additionally, inasmuch as claim 17 depends, either directly or indirectly from an allowable independent claim 14, the applicant submits that claim 17 is itself allowable. For at least these reasons, the applicant respectfully requests the Office to withdraw its rejection of claim 17, and allow claim 17 to issue.

Claims 18-20

Claims 18-20 depend either directly or indirectly from allowable independent claim 14. For least this reason, the applicant submits that claims 18-20 are themselves allowable, and respectfully requests the Office to withdraw its rejection of claims 18-20, and allow these claims to issue.

Claim 21

Claim 21 recites a second means for controlling system memory during a power savings state, wherein the second means includes means for holding an output terminal at a high

impedance during operational state and means for providing a first logic level through the output terminal during the power savings state.

The applicant submits that Baweja does not disclose holding a high impedance on output terminal during operational state, and providing a first logic level through that same terminal during a power savings state. For example, if Baweja were to hold the output CKE 330 (Fig. 3) or CKE 260 (Fig. 2) at a high impedance during an operational state, then signal SDCKE 240 from first memory controller 210 could not be used to control system memory during the operational state.

For at least this reason, the applicant submits that Baweja does not teach or suggest each and every element recited in independent claim 21, and requests the Office to withdraw its rejection of claim 21, and allow claim 21 to issue.

Claim 22-23

Claims 22-23 depend either directly or indirectly from allowable independent claim 21. For at least this reason, the applicant submits that claims 22-23 are themselves allowable, and respectfully requests the Office to withdraw its rejection of claims 22-23, and allow these claims to issue.

Claim 24-25

Claim 24 recites an integrated circuit responsive to a first operational state of the computer system to place an output terminal at a high impedance level and responsive to a power savings state of the computer system to supply the first logic level on the output terminal.

The applicant submits that Baweja does not disclose holding a high impedance on output terminal in response to an operational state, and supplying a first logic level through that same terminal in response to a power savings state.

For at least this reason, the applicant submits that Baweja does not teach or suggest each and every element recited in independent claim 24, and requests the Office to withdraw its rejection of claim 24 and allow claim 24 to issue. Inasmuch as claim 25 depends from allowable

independent claim 24, the applicant further requests Office to withdraw its rejection of claim 25 and allow claim 25 to issue.

Claim 31

Claim 31 recites an apparatus wherein a reset signal coupled to the second circuit, when asserted, causes the second circuit to keep the memory control signal at the logic level to maintain the memory in a self refresh state. The applicant submits that the Office has not cited a specific portion of Baweja that teaches or suggests using a reset signal to keep the memory control signal at a logic level necessary to maintain the memory in a self refresh state. For at least this reason, the applicant respectfully requests the Office to withdraw its rejection of claim 31, and allow claim 31 to issue.

Claim Rejections under 35 USC Section 103

Claims 32 and 33

Claims 32 and 33 were rejected under 35 USC section 103(a) as being unpatentable over Baweja. Inasmuch as claims 32 and 33 depend from allowable independent claim 31, which the applicant submits is allowable for the reasons given above, claims 32 and 33 are themselves allowable. The applicant, therefore, respectfully requests Office to withdraw its rejection of claims 32 and 33, and allow claims 32 and 33 to issue.

CONCLUSION

In summary, claims 1-27 and 31-33 are in the case. All claims are believed to be allowable over the art of record, and a Notice of Allowance to that effect is respectfully solicited. Nonetheless, if any issues remain that could be more efficiently handled by telephone, the Examiner is requested to call the undersigned at the number listed below.

CERTIFICATE OF MAILING OR TRANSMISSION

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Edward J. Marshall 2/17/04
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